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(11) Publication number:

0 552 726 A2

(12)

EUROPEAN PATENT APPLICATION

(21) Application number: 93100789.2

(61) Int. Cl. 5: G01D 5/244

(22) Date of filing: 20.01.93

(30) Priority: 21.01.92 JP 8469/92

(71) Applicant: CANON KABUSHIKI KAISHA
30-2, 3-chome, Shimomaruko, Ohta-ku
Tokyo(JP)

(43) Date of publication of application:
28.07.93 Bulletin 93/30

(72) Inventor: Eguchi, Tadashi, c/o Canon
Kabushiki Kaisha
30-2, 3-chome, Shimomaruko
Ohta-ku, Tokyo 146(JP)

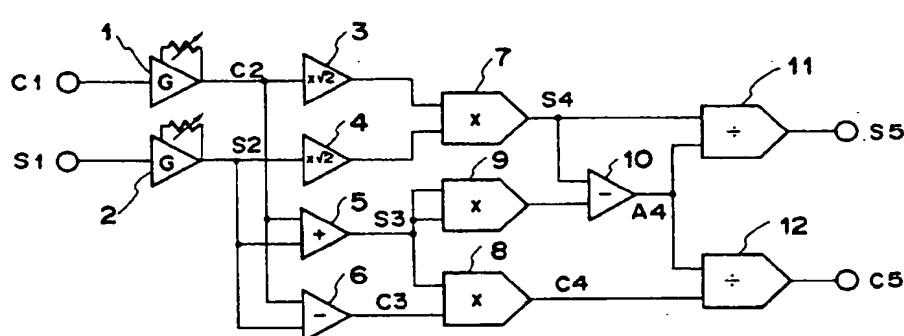
(84) Designated Contracting States:
DE FR GB IT

(74) Representative: Tiedtke, Harro, Dipl.-Ing.
Patentanwälte Tiedtke-Bühling- Kinne &
Partner Bavariaring 4 Postfach 20 24 03
W-8000 München 2 (DE)

(54) Signal processing apparatus and method, and displacement detecting apparatus using the same.

(57) In a signal processing apparatus and method, original two-phase signals each having the possibility of amplitude fluctuation are received by an input portion. From the original two-phase signals received by the input portion, new two-phase signals are formed by a signal processing portion. The signal processing portion forms an intermediate stage two-phase signal and a phase component eliminated signal having the phase components of the original signals eliminated therefrom in parallel from the original two-phase signals, and eliminates the fluctuation component of amplitude by the offsetting process of respective ones of the two-phase signals and the phase component eliminated signal to thereby form the new two-phase signals. The new two-phase signals have a predetermined phase relation with the original two-phase signals. The new two-phase signals are output from an output portion. This specification also discloses a displacement detecting apparatus using such signal processing apparatus.

FIG. 3



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BACKGROUND OF THE INVENTIONField of the Invention

5 This invention relates to signal processing for enhancing detection resolution on the basis of a periodic signal obtained in a displacement detecting apparatus such as an encoder or an interferometer.

Related Background Art

10 In an optical incremental type rotary encoder or linear encoder, the displacement or the direction of movement of a moving object is detected by the use of two sine wave signals differing in phase (two-phase sine wave signals, in other words, a sine wave signal and a cosine wave signal) obtained from light receiving means. There is known a technique of producing signals differing in phase from said sine wave signal and said cosine wave signal by a signal interpolating process and increasing the number of divided pulses to thereby enhance detection resolution.

15 Figure 1 of the accompanying drawings is a construction diagram showing an example of the signal processing means, and Figure 2 of the accompanying drawings shows signal waveforms in the various circuit portions of Figure 1. In Figure 1, the reference numerals 21 and 22 designate input terminals to which a sine wave signal S1 and a cosine wave signal C1 are input. That is, in contrast with a signal a (sine wave) from the input terminal 21, a signal b (cosine wave) having a phase difference of 90° is input from the input terminal 22. Also, a signal c given a phase difference of 180° with respect to the signal a is obtained in an inverting circuit 23. These three signals a, b and c are suitably weight-added by resistors R, and a sine wave signal of any phase (angle) is interpolated. In Figure 1, all the resistors R are of the same value and signals d and e of phase differences 45° and 135°, respectively, are obtained.

20 These signals are converted into rectangular waves by four comparators 24, 25, 26 and 27, but usually the inputs of the comparators are given a hysteresis so that the comparators may not cause chattering by the influence of the noise at this time. A pulse circuit 28 is means for obtaining rectangular wave signals of two phases having a phase difference of 90° therebetween. In this manner, signals of higher resolution can be obtained from the sine wave signal and cosine wave signal obtained from the light receiving means.

25 Also, discretely from this, an attempt has been made to provide an electrical interpolation method using a combination of an analog multiplier and said resistance division as shown in Japanese Laid-Open Patent Application No. 3-99219, or to output interpolation data in a memory with a value which is obtained by A/D-converting two-phase sine wave signals as an address, thereby obtaining high resolution.

30 However, the above-described technique of interpolating an original signal from the phase information of the two-phase sine wave signals of the displacement detecting apparatus such as the encoder or the laser interferometer and enhancing the resolution has suffered from the following problems.

35 Generally in the encoder or the interferometer, there is a case where the quantity of reflected light, the quantity of transmitted light or the interference state varies with the movement of an object to be measured, whereby the magnitude of the amplitude of a periodic signal obtained is varied. In such case, the following inconveniences occur:

- 40 (1) When phase division is to be effected by the construction as shown in Figure 1, if the amplitudes of the input signals S1 and C1 vary, the phase with which the rectangular wave is output will be varied by a hysteresis voltage as indicated by dotted lines in Figure 2;
- 45 (2) When two-phase sine wave signals are to be directly A/D-converted, if the signals become small, the quantization error of the A/D converter will become unnegligible and division accuracy will be reduced; and
- 50 (3) When as shown in the aforementioned Japanese Laid-Open Patent Application No. 3-99219, an attempt is made to enhance the resolution by the use of the analog multiplier, the amplitude of the output of the multiplier is proportional to the square of the amplitude of the two-phase sine wave of the original signal and therefore, if for example, the amplitude of the original signal becomes 1/2, the output of the multiplier will become 1/4 and S/N will be extremely reduced.

SUMMARY OF THE INVENTION

55 The present invention has been made to solve the above-noted problems and an object thereof is to provide a technique whereby even if a fluctuation occurs to the amplitude of a reference periodic signal input, signal processing for higher resolution can be effected highly accurately without being affected by the fluctuation.

Other objects of the present invention will become apparent from the following description of some embodiments of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

- 5 Figure 1 is a construction diagram of a signal circuit according to the prior art.
- Figure 2 shows signal waveforms in the circuit of Figure 1.
- Figure 3 is a construction diagram of a signal circuit according to an embodiment of the present invention.
- 10 Figure 4 is a construction diagram of a signal circuit according to another embodiment of the present invention.
- Figure 5 is a construction diagram of an encoder using the principle of light interference.
- Figure 6 is a construction diagram of a driving system having the encoder.
- Figure 7 is a construction diagram of a servowriter system for a hard disk.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A signal processing apparatus according to an embodiment which will hereinafter be described has means for inputting a sine wave signal and a cosine wave signal which become a reference, calculating means for creating a sine wave signal of a frequency natural number times as high as the frequency of said reference signals, calculating means for creating a cosine wave signal of a frequency natural number times as high as the frequency of said reference signals, and regulating means for regulating the amplitudes of said created sine wave signal and cosine wave signal of the frequency natural number times as high as the frequency of said reference signals so as to become constant irrespective of the fluctuation of the amplitude of said reference signals.

The invention will hereinafter be described in detail with respect to some embodiments thereof shown in the drawings. Figure 3 is a construction diagram of the signal processing apparatus of the displacement detecting apparatus of the present invention. The reference numerals 1 and 2 designate amplitude regulating means, the reference numerals 3 and 4 denote $\sqrt{2}$ time amplifiers, the reference numeral 5 designates an adder, the reference numeral 6 and 10 denote subtractors, the reference numerals 7, 8 and 9 designate analog multipliers, and the reference numerals 11 and 12 denote dividers.

The amplitudes of periodic signals of two phases (sine wave and cosine wave) obtained in a displacement detecting mechanism or the like are not always coincident with each other in a state in which there is no fluctuation in the amplitudes, and two signals C1 and S1 input from input terminals are expressed by the following equations:

$$C1 = P_1 \cos\omega t \quad (1)$$

$$S1 = P_2 \sin\omega t, \quad (2)$$

40 where P_1 and P_2 are the amplitudes of the two-phase sine waves.

The amplitude regulating means 1 and 2 regulate the amplification factors of the input two-phase sine waves C1 and C2, respectively, by variable resistors to thereby obtain two-phase sine wave signals C2 and S2 of the same amplitude P.

$$45 \quad C2 = P \cos\omega t \quad (3)$$

$$S2 = P \sin\omega t \quad (4)$$

50 From these signals, a sum signal S3 and a difference signal C3 are produced by the adder 5 and the subtractor 6, respectively.

$$\begin{aligned} S_3 &= P \cos \omega t + P \sin \omega t \\ &= \sqrt{2} P \sin (\omega t + \pi/4) \quad \dots (5) \end{aligned}$$

5

$$\begin{aligned} C_3 &= P \cos \omega t - P \sin \omega t \\ &= \sqrt{2} P \cos (\omega t + \pi/4) \quad \dots (6) \end{aligned}$$

10 The multiplier 8 effects the multiplication of S_3 and C_3 , and the output C_4 thereof is

$$\begin{aligned} C_4 &= 2P^2 \sin (\omega t + \pi/4) \cdot \cos (\omega t + \pi/4) \\ &= P^2 \sin (2\omega t + \pi/2) \\ &= P^2 \cos 2\omega t. \quad \dots (7) \end{aligned}$$

20 The multiplier 7 effects the multiplication of outputs obtained by amplifying C_2 and S_2 by the $\sqrt{2}$ time amplifiers 3 and 4, respectively, and the output S_4 thereof is

$$\begin{aligned} S_4 &= 2P^2 \sin \omega t \cdot \cos \omega t \\ &= P^2 \sin 2\omega t. \quad \dots (8) \end{aligned}$$

30 On the other hand, a signal A_4 obtained by subtracting S_4 from the square signal of S_3 by the subtractor 10 is

$$\begin{aligned} A_4 &= (P \cos \omega t + P \sin \omega t)^2 - 2P^2 \sin \omega t \cdot \cos \omega t \\ &= P^2. \quad \dots (9) \end{aligned}$$

40 Outputs S_5 and C_5 obtained by dividing S_4 and C_4 by A_4 by the use of the dividers 11 and 12, respectively, are

40

$$C_5 = \cos 2\omega t \quad (10)$$

$$S_5 = \sin 2\omega t. \quad (11)$$

45 As will be seen from equations (10) and (11), even if the amplitude of the original signal varies and the amplitude P of the two-phase sine wave signals C_2 and S_2 varies, it will not affect the finally obtained periodic signals C_5 and S_5 of double frequency.

The above-described circuit construction is not restrictive, but other forms are also conceivable. Figure 4 shows a modification of the above-described construction, and in Figure 4, the same reference numerals 50 as those in Figure 3 designate the same members. The reference numerals 13, 14 and 15 denote analog multipliers, the reference numeral 16 designates an adder, and the reference numeral 17 denotes a subtractor. In the construction of Figure 4, as compared with the construction of Figure 3, the calculating method for obtaining the signals A_4 and C_4 differs, but the signals obtained are identical and therefore, the same operational effect as that of the embodiment of Figure 3 is obtained.

55 Also, if the phase delay by the amplifier poses no problem, one of the $\sqrt{2}$ time amplifiers 3 and 4 may be omitted and the other may be replaced by a two-time amplifier.

The above-described/processing procedure may be summed up as follows.

(1) The square signal A4 of the amplitude of the input sine wave signal S2 and cosine wave signal C2 is obtained by the use of the analog multiplier, the adder or the like. This square signal includes the fluctuation information of the amplitude of the reference signal. The phase component is eliminated.

5 (2) The signals S4 and C4 of a frequency (resolution) double the frequency of the reference signal are obtained by the use of the analog multipliers

(3) The sine wave signal S4 and cosine wave signal C4 of double frequency are each divided by said square signal A4 by the use of the dividers to thereby offset the fluctuations of the amplitudes and create the sine wave signal S5 and cosine wave signal C5 of which the frequency is constantly double.

As described above, the output of the circuit of the present construction is not affected by the fluctuation of the amplitude of the input signal, and this leads to the following advantages when this output signal is electrically interpolated as a two-phase sine wave signal:

(1) When the two-phase sine wave signal is read in by the A/D converter, any reduction in interpolation accuracy by the quantization error of the A/D converter can be prevented;

15 (2) In the case of a system in which the two-phase sine wave signal is read in by the A/D converter and with the data thereof as addresses, the phase information in a memory is called out, the amplitude is constant and therefore, the addresses may be few, that is, the capacity of the memory may be small;

(3) When phase division is effected, any extreme reduction in S/N ratio does not occur in spite of the multiplier being used;

20 (4) Even if use is made of the analog multiplier as shown in Japanese Laid-Open Patent Application No. 3-99219, little or no reduction in S/N ratio occurs; and

(5) The two-phase signals S4 and C4 at the intermediate stage and the signal A4 from which the phase component has been eliminated are formed in parallel and by the division of these, the final two-phase signal is formed and therefore, the follow-up delay or the like as when feedback or the like is effected does not occur.

25 Now, the signal processing circuit has been described above, and this signal processing circuit may preferably used in an apparatus such as a displacement detecting apparatus or a laser length measuring machine. As an example, the construction of a displacement detecting apparatus such as a linear encoder or a rotary encoder having the above-described signal processing circuit is shown in Figure 5.

A light beam emitted from a coherent light source 101 such as a semiconductor laser is split into two 30 light beams by a beam splitter 102, and the two light beams are incident on a single-point position on a diffraction grating 103 which is a movement amount measuring slit formed on a movable scale plate or a rotatable disk plate. High-order diffracted lights created from the diffraction grating 103 toward a reflecting optical system 104 by the incidence of the light beams, here ± 1 st-order diffracted lights, are both reflected by the reflecting optical system 104 and are again incident on substantially the same position on the 35 diffraction grating 103. The reflecting optical system 104 forms a so-called cat's eye optical system. ± 1 st-order re-diffracted lights created there by the re-incidence return along substantially the same optical path as that during the incidence. Interference lights formed by these ± 1 st-order re-diffracted lights are made into periodic signals of two phases having a phase difference of 90° therebetween by a polarizing beam splitter 104' and a deflecting plate and are detected by photodetectors 106 and 107, respectively. As regards sine 40 and cosine detection signals obtained by these photodetectors 106 and 107, harmonic signals are produced to enhance detection resolution by a processing circuit 108 having the signal processing circuit shown in Figure 3 or 4, and the zero cross point of the waveforms of the created signals is detected to thereby obtain divided pulses, which are output as detection pulses conforming to the displacement of the diffraction grating. Thus, a number of detection pulses conforming to the amount of displacement (the amount of 45 movement or the amount of rotation) of the diffraction grating relative to the incident light beam are output from the output terminal of the processing circuit 108. Further, the direction of rotation or the direction of movement is also detected by the utilization of the phase difference between the two signals.

Figure 6 shows an example of the use of the above-described encoder, and is a system construction diagram of a driving system using the encoder. An encoder unit 111 is connected to the driving output portion of driving means 110 having a drive source such as a motor, an actuator or an engine, or to a moving portion for an object driven, and detects the driven state such as the amount and speed of rotation or the amount and speed of movement. This encoder unit has the signal processing circuit described in connection with Figure 3 or 4. The detection output from the encoder unit 111 is fed back to control means 112, and a driving signal is transmitted to the driving means 110 so that a condition set by setting means 113 may be brought about in the control means 112. By such a feedback system being constituted, the driving condition set by the setting means 113 can be kept. Such a driving system can be widely applied to a business machine such as a typewriter, a printer, a copying machine or a facsimile apparatus, a video instrument such as a camera or a video recorder, a recording apparatus, a robot, a machine tool, a

manufacturing apparatus and further, any apparatus having driving means.

Figure 7 shows a specific example using such driving system, and particularly shows the general construction of the servo-writer system of a hard disk. In Figure 7, the reference numeral 200 designates the surface of a magnetic disk rotated by driving means, not shown, the reference numeral 201 denotes a motor such as a stepping motor capable of highly accurate rotation, the reference numeral 203 designates the motor shaft of the motor 201, the reference numeral 204 denotes an arm portion directly mounted on the motor shaft 203, and the reference numeral 205 designates a track signal writing head attached to the tip end of the arm portion 204. With such construction, the writing head 205 is moved diametrically on the surface 200 of the magnetic disk by the rotation of the motor 201. The reference numeral 202 denotes the rotary encoder described above. The rotary encoder 202 is mounted on the rotary shaft of the motor 201 and detects the amount of rotation of the motor 201.

On the other hand, the reference numeral 206 designates a divider having the signal processing circuit described in connection with Figure 3 or 4. The divider 206 electrically divides the detection output of the encoder 202 and enhances the detection resolving power. The reference numeral 207 denotes a counter for counting the detection pulses from the divider 206. The reference numeral 208 designates a controller for synthetically controlling the system. The controller 208 has a CPU, a DSP, etc. The reference numeral 209 denotes a motor driver for driving the motor 201 on the basis of the command of the controller 208. The motor driver 209 has a D/A converter, etc. The reference numeral 210 designates a host computer for setting the operation of the system.

The controller 208, on the basis of the detection by the encoder obtained from the counter 207, gives a command to the motor driver 209 so that the operation of the system may become the operation as set by the host computer 210, and the motor driver 209 drives the motor 201 to thereby move the writing head 205 attached to the tip end of the arm portion 204 diametrically on the surface 200 of the magnetic disk and accurately shift it to a predetermined track position. On the basis of a signal from a circuit, not shown, the writing head 205 writes a track signal onto the surface 200 of the magnetic disk.

According to the present invention, even if any fluctuation of the amplitude of the input reference signal occurs, the signal processing for higher resolution can be effected without being affected by it.

In a signal processing apparatus and method, original two-phase signals each having the possibility of amplitude fluctuation are received by an input portion. From the original two-phase signals received by the input portion, new two-phase signals are formed by a signal processing portion. The signal processing portion forms an intermediate stage two-phase signal and a phase component eliminated signal having the phase components of the original signals eliminated therefrom in parallel from the original two-phase signals, and eliminates the fluctuation component of amplitude by the offsetting process of respective ones of the two-phase signals and the phase component eliminated signal to thereby form the new two-phase signals. The new two-phase signals have a predetermined phase relation with the original two-phase signals. The new two-phase signals are output from an output portion. This specification also discloses a displacement detecting apparatus using such signal processing apparatus.

Claims

1. A signal processing apparatus, comprising:
 - an input portion for receiving original two-phase signals each having possibility of amplitude fluctuation;
 - a signal processing portion for forming new two-phase signals from the original two-phase signals received by said input portion, said signal processing portion forming an intermediate stage two-phase signal and a phase component eliminated signal having the phase components of said original signals eliminated therefrom in parallel from said original two-phase signals, and eliminating the fluctuation component of amplitude by the offsetting process of respective ones of said two-phase signals and said phase component eliminated signal to thereby form said new two-phase signals, said new two-phase signals having a predetermined phase relation with said original two-phase signals; and
 - an output portion for outputting said new two-phase signals.
2. A signal processing apparatus according to Claim 1, wherein said signal processing portion has a first circuit for regulating the amplitudes of said original two-phase signals and forming two-phase signals of the same amplitude, a second circuit for forming the sum signal of and the difference signal between said two-phase signals of the same amplitude, a third circuit for forming the multiplied signal of said sum signal and said difference signal as a first signal of said intermediate stage two-phase signal, a fourth circuit for forming the multiplied signal of amplified signals $\sqrt{2}$ times as great as respective ones

of said sum signal and said difference signal as a second signal of said intermediate stage two-phase signal, a fifth circuit for forming the difference signal between said second signal and the square signal of said sum signal as said phase component eliminated signal, and a sixth circuit for dividing said first signal and said second signal by said phase component eliminated signal and forming said new two-phase signals.

5 3. A signal processing apparatus according to Claim 1, wherein said signal processing portion has first means for forming from said original two-phase signals a phase signal of a frequency double the frequency of one of said original two-phase signals, second means for forming from said original two-phase signals a phase signal of a frequency double the frequency of the other of said original two-phase signal, third means for forming said phase component eliminated signal from said original two-phase signals, and fourth means for dividing said phase component eliminated signal by said two-phase signals to thereby form said new two-phase signals.

10 4. A signal processing method, comprising:
 the reception of original two-phase signals each having the possibility of amplitude fluctuation;
 the formation of new two-phase signals from said received original two-phase signals, the formation of said new two-phase signals being executed by the parallel formation of an intermediate stage two-phase signal and a phase component eliminated signal having the phase components of said original signals eliminated therefrom from said original two-phase signals, and the eliminating process of the fluctuation component of amplitude by the offsetting process of respective ones of said two-phase signals and said phase component eliminated signal, said new two-phase signals having a predetermined phase relation with said original two-phase signals; and
 the output of said new two-phase signals.

25 5. A signal processing method according to Claim 4, wherein the formation of said new two-phase signals has:
 the first step of regulating the amplitudes of said original two-phase signals and forming two-phase signals of the same amplitude;
 the second step of forming the sum signal of and the difference signal between said two-phase signals of the same amplitude;
 the third step of forming the multiplied signal of said sum signal and said difference signal as a first signal of said intermediate stage two-phase signal;
 the fourth step of forming the multiplied signal of amplified signals $\sqrt{2}$ times as great as respective ones of said sum signal and said difference signal as a second signal of said intermediate stage two-phase signal;
 the fifth step of forming the difference signal between said second signal and the square signal of said sum signal as said phase component eliminated signal; and
 the sixth step of dividing said first signal and said second signal by said phase component eliminated signal and forming said new two-phase signals.

35 6. A signal processing method according to Claim 5, wherein the formation of said new two-phase signals has:
 the step of forming from said original two-phase signals a phase signal of a frequency double the frequency of one of said original two-phase signals;
 the step of forming from said original two-phase signals a phase signal of a frequency double the frequency of the other of said original two-phase signals;
 the step of forming said phase component eliminated signal from said original two-phase signals; and
 the step of dividing said phase component eliminated signal by said two-phase signals to thereby form said new two-phase signals.

40 7. A displacement detecting apparatus, comprising:
 a sensor portion for outputting the displacement of a movable portion as two-phase signals corresponding to said displacement; and
 a signal processing portion for forming new two-phase signals from the two-phase signals from said sensor portion, said signal processing portion forming an intermediate stage two-phase signal from the two-phase signals from said sensor portion and a signal having the phase component of an original

signal eliminated therefrom in parallel, and dividing respective ones of said two-phase signals and said phase component eliminated signal to thereby eliminate the fluctuation component of amplitude and form said new two-phase signals, said new two-phase signals having a predetermined phase relation with the two-phase signals from said sensor portion;

5 the displacement information of said movable portion being detected by said new two-phase signals.

8. A displacement detecting apparatus according to Claim 7, wherein said sensor portion has a grating interferometer.

10 9. A displacement detecting apparatus according to Claim 8, wherein said grating interferometer is provided on a motor, and the amount of rotation of said motor as the displacement information is detected by said new two-phase signals.

15 10. A displacement detecting apparatus according to Claim 7, further having control means for controlling the displacement of said movable portion.

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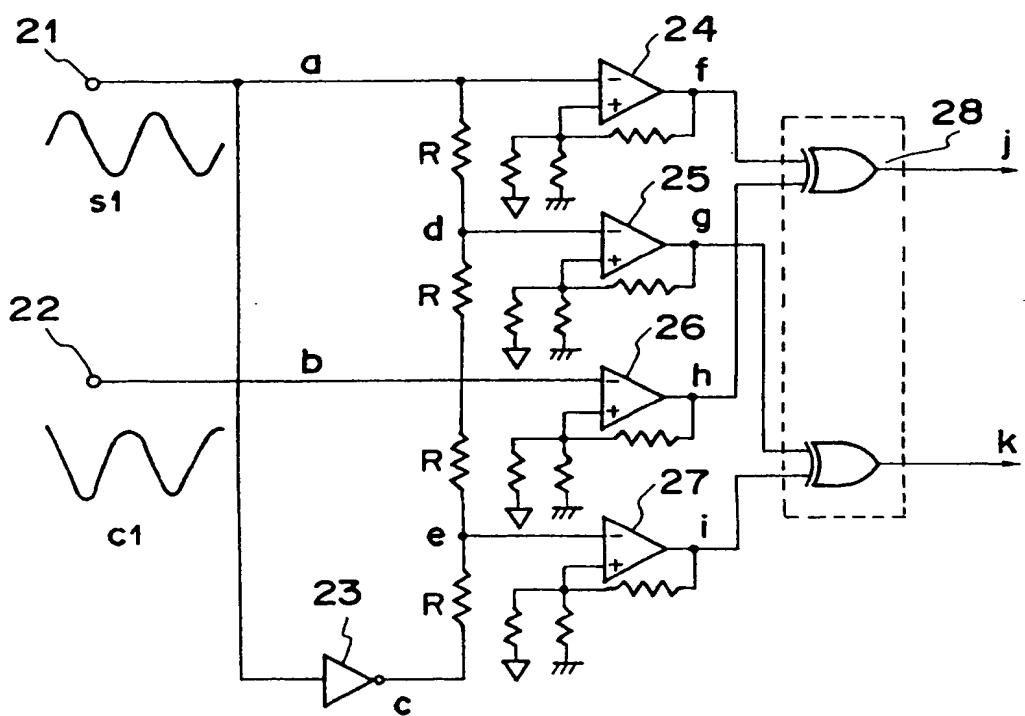
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FIG. 1
PRIOR ART



F I G. 2

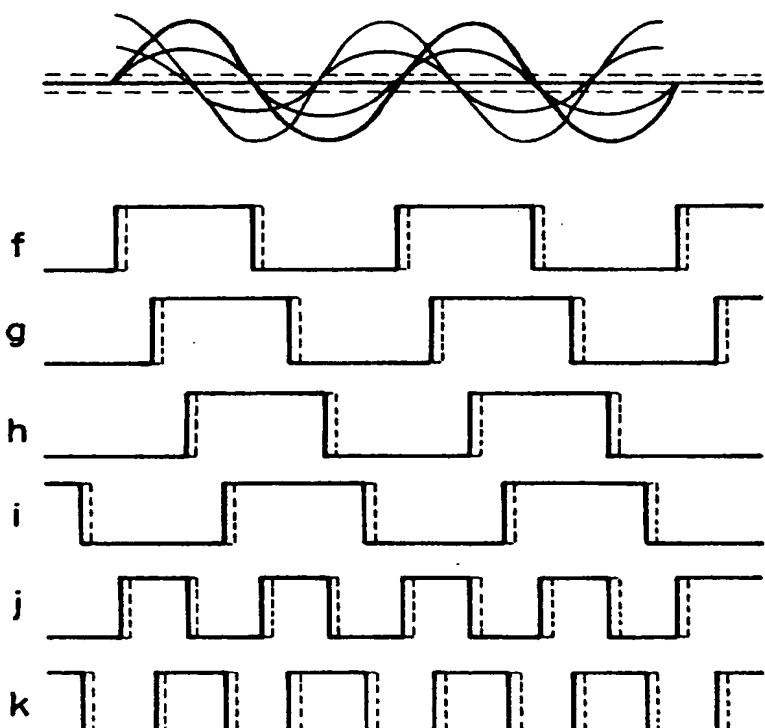


FIG. 3

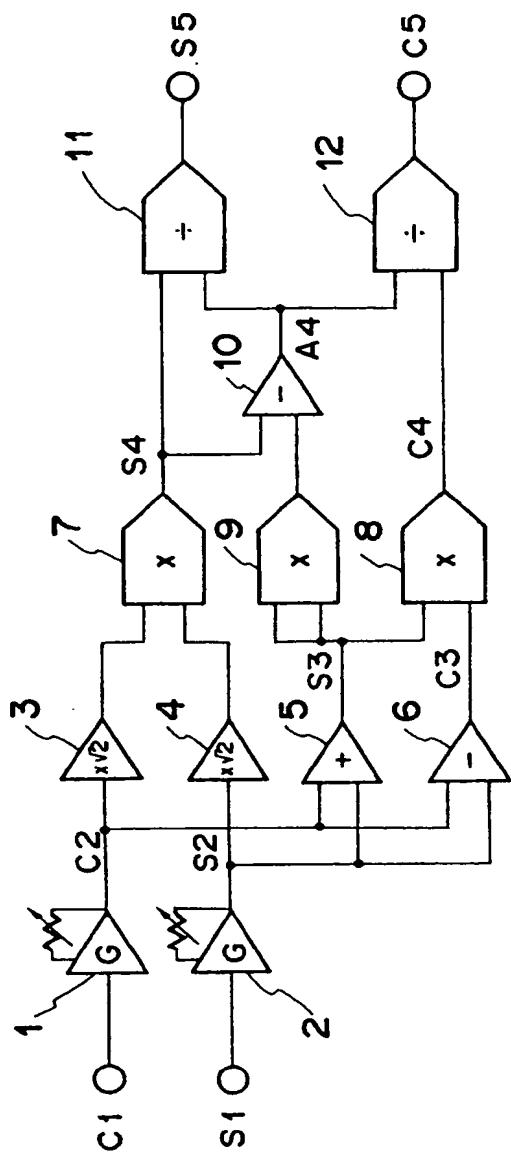


FIG. 4

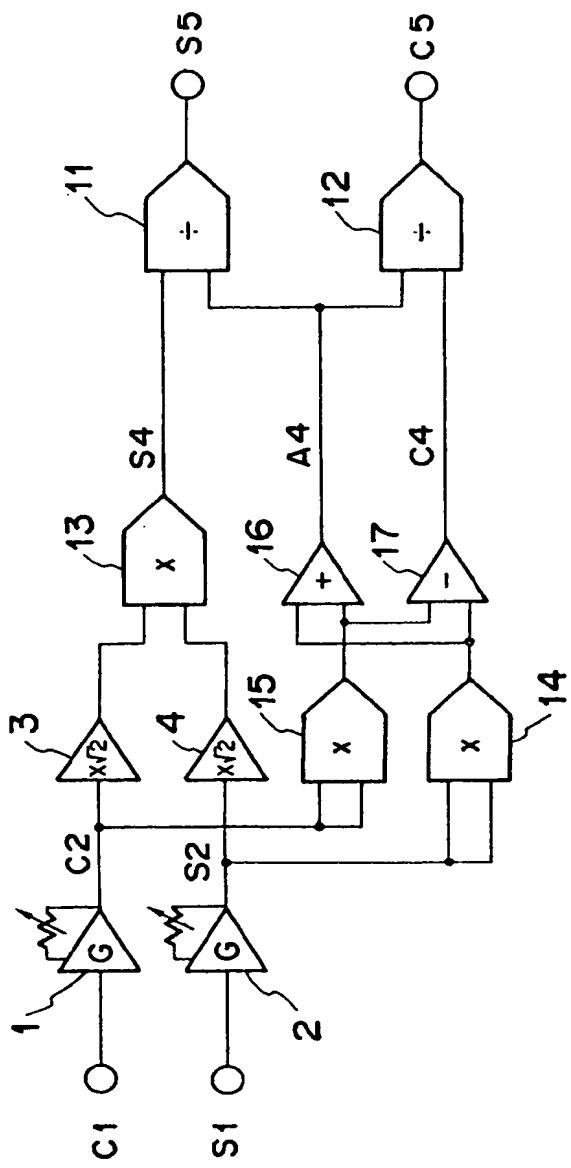
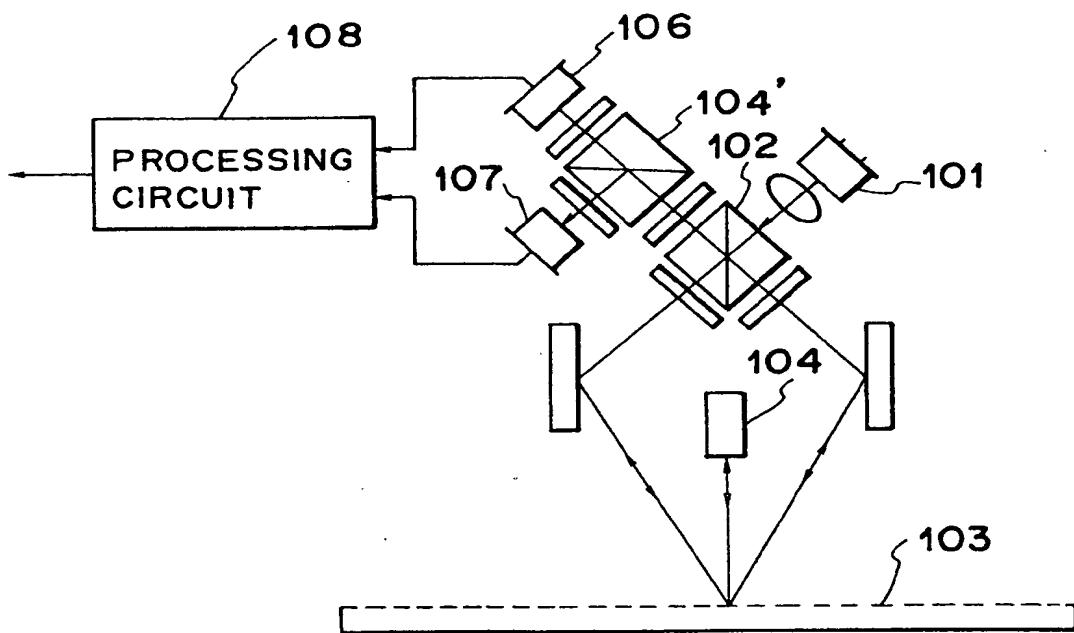


FIG.5



F I G. 6

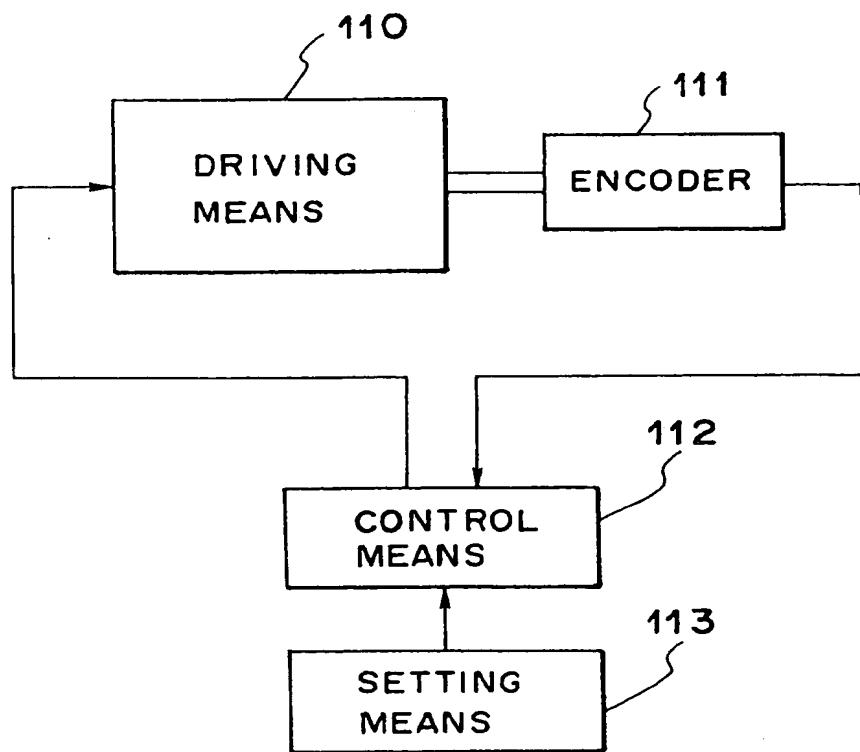
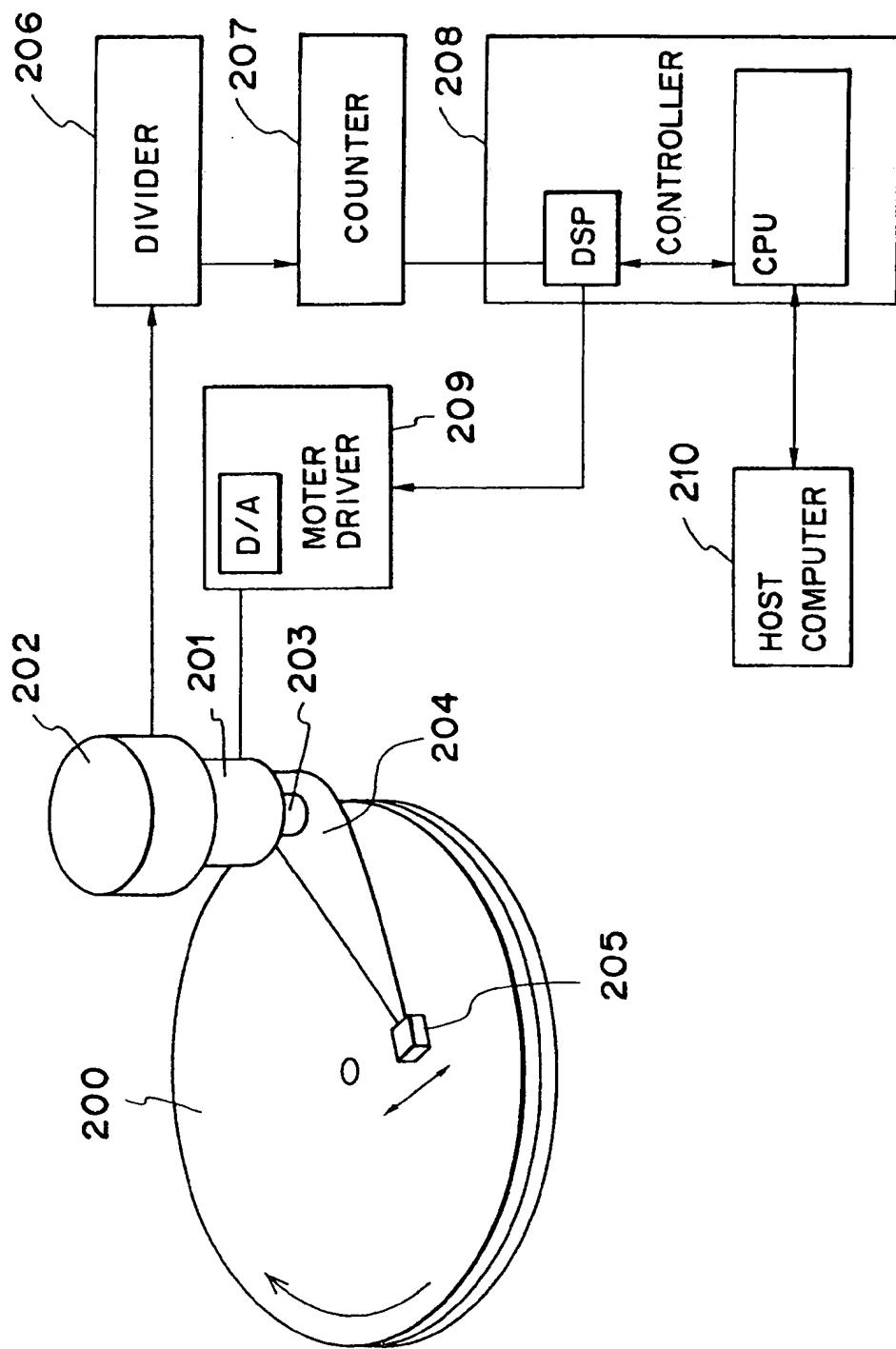


FIG. 7





(19)

Europäisches Patentamt

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(11)

EP 0 552 726 A3

(12)

EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
24.07.1996 Bulletin 1996/30

(51) Int. Cl.⁶: **G01D 5/244**, G01D 5/245,
G01D 5/36

(43) Date of publication A2:
28.07.1993 Bulletin 1993/30

(21) Application number: 93100789.2

(22) Date of filing: 20.01.1993

(84) Designated Contracting States:

(30) Priority: 21.01.1992 JP 8469/92

(71) Applicant: CANON KABUSHIKI KAISHA
Tokyo (JP)

(72) Inventor: Eguchi, Tadashi,
c/o Canon Kabushiki Kaisha
Ohta-ku, Tokyo 146 (JP)

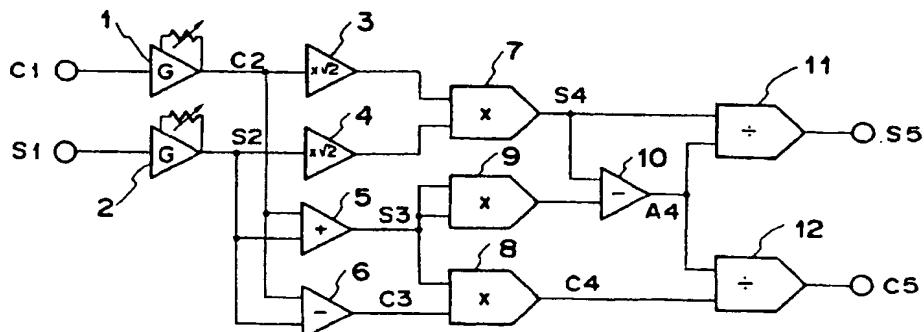
(74) Representative: **Tiedtke, Harro, Dipl.-Ing.**
Patentanwaltsbüro
Tiedtke-Bühling-Kinne & Partner
Bavariaring 4
80336 München (DE)

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FIG. 3





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 10 0789

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int.CI5)						
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim							
X	EP-A-0 377 045 (FANUC) * abstract; figure 1 *	1,4,7	G01D5/244						
Y		2,3,5,6	G01D5/245						
D,Y	PATENT ABSTRACTS OF JAPAN vol. 015, no. 287 (P-1229), 22 July 1991 & JP-A-03 099219 (TAMAGAWA), 24 April 1991, * abstract *	2,3,5,6	G01D5/36						
			TECHNICAL FIELDS SEARCHED (Int.CI5)						
			G01D						
<p>The present search report has been drawn up for all claims</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">Place of search</td> <td style="width: 33%;">Date of completion of the search</td> <td style="width: 34%;">Examiner</td> </tr> <tr> <td>THE HAGUE</td> <td>21 May 1996</td> <td>Lloyd, P</td> </tr> </table>				Place of search	Date of completion of the search	Examiner	THE HAGUE	21 May 1996	Lloyd, P
Place of search	Date of completion of the search	Examiner							
THE HAGUE	21 May 1996	Lloyd, P							
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</p>									